TECHNICAL HIGHLIGHTS

- Compliant with Pipe 5.x
- The flexible and easy user interface
- Compliant with ATS Specification
- Compliant with SR-10v Specifications

* compliant with CXS specification for CCIX packets

* Support for CCIX packets

- Supports X32, X16, X8, X4, X2, X1 Lanes
- Simple Clocking architecture
- Supports both PIPE Serdes and non-Serdes architecture.
- Inbuilt configurable address translator.
- 32 Physical and 512 virtual functions supported (configurable)
- EP/ RC/ DM/ Switch configurations
- Highly configurable, robust DMA architecture
- Compliant with AMBA Interfaces Latest versions
- Compliant with PCI Express 5.X (32 GT/s) 4.X (16 GT/s) , 3.X (8GT/s)
- Support for single and multi-link PCIE connectivity
- 512b Controller architecture and 64b PIPE interface for very high performance
- LTR, AER, OBFF, MSI, MSI-X, PTM, ARI, ERC, Crosslink and all features supported
- Required features can be turned on and off at the core generation phase
  for an optimized gate count controller
- Checked with multiple PHY vendors, Tester units, Multiple VIPs.

PRIMESOC Technologies
(Total IP and Services solution provider)

E-mail
support@primesocvlsi.com

Website
www.primesocvlsi.com